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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/256,643	02/23/1999	LEONARD FORBES	303.324US2	1086

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TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/256,643	Applicant(s) FORBES ET AL.	
	Examiner Michael M Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23,24,26,29-33 and 36-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23,24,26,29-32,36-46,48-61,63-66,68,69 and 71-74* is/are rejected.

7)☒ Claim(s) *33,47,62,67,70 and 75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *21* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's response filed on January 04, 2002. Claims 34-35 were canceled. Claims 21,23-24,26,29-33,36-75 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 21,23-26,29-32,36-46,48-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain (4,473,836) taken with Halvis et al (5,369,040).

Chamberlain teaches a method for forming a transistor (Figs 2,4; columns 3-6 comprising: forming diffused regions D1,D2 that respectively function as a source region and drain region in a semiconductor silicon substrate (col 3, lines 11-27), wherein a channel region being between the source and drain regions; forming an insulating layer 13 on the channel region; forming a layer of polysilicon material; and removing portions of the insulating layer and the layer of gate material 14 by patterning and etching to form a gate on the substrate

Chamberlain lacks to form the gate of silicon carbide compound.

However, *Halvis* et al teach (at col 4, lines 10-15; cols 3-4), rather using polysilicon gate, using silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5. for forming a gate on the gate insulating,layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Chamberlain with the gate of silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 as taught by Halvis et al. This is because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity.

Regarding other limitations including deposition techniques, for example, in claim 40, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide.

Implanting dopant into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

2. Claims 21,23-24,26,29-32,36-46,48-59,60-61,63-66,68-69,71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al (5,449,941) taken with Halvis et al (5,369,040).

Yamazaki et al teaches a method for forming a MOS transistor for memory cell (Figs 1A-1D; 2A-2D; col 4, lines 12-15; lines 27-60; col 3,lines 66-68) comprising: forming a source region and drain region in a semiconductor silicon substrate 201 (Fig 2A; col 3, lines 35-68), wherein a channel region being between the source and drain regions 203,204; forming an insulating layer 206/207 on the channel region; forming a floating gate 208 by patterning and etching a layer of gate material; forming an intergate dielectric layer 209; and forming a control gate 210 over the floating gate 208.

Yamazaki lack to form the floating gate of silicon carbide compound.

However, *Halvis* et al teach (at col 4, lines 10-15; cols 3-4), rather using polysilicon gate, using silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5. for forming a gate on the gate insulating layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 as taught by Halvis et al. This is because of the desirability to improve response, to improve

quantum efficiency, and to improve performance and light sensitivity. Regarding other limitations including deposition techniques, for example, in claim 40, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting dopant into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

3. Claims 21,23-24,26,29-32,36-46,48-59,60-61,63-66,68-69,71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halvis et al (5,369,040) taken with Tohyama (5,858,811) and Chamberlain (4,473,836).

Halvis et al teaches a method for forming a semiconductor device (Figs 4A-4C; cols 3-4) comprising: forming an insulating layer 32 on the channel region; forming a floating gate 38 by patterning and etching a layer of gate material 33 (figs 4A-4B; col 3, line 61 through col 4); forming an intergate dielectric layer 42 by oxidizing; and forming a control gate 50 over the floating gate 38 with the intergate dielectric layers 42 therebetween (Fig 4C).

Halvis lack to remove portion of the insulating layer during formation of the gate 38, and lacks to show source and drain regions.

However, *Tohyama* et al alternatively teach (at Fig 1 to 4; col 1-3, cols 5-6) either removing portions of the first insulating layer 4 (Fig 3C; col 2, lines 40-63) and the layer of gate material 6 to form a gate 8, or not removing a portion of the first insulating layer 4 (Figs 1C-1D); forming an interlayer dielectric layer; and forming a second gate 13, wherein the gate layer is doped with n-type or p-type impurities (col 6, lines 20-25). Chamberlain teaches (at col 3, lines 20-27) a photodetector as of Halvis, wherein diffused regions functioned as source and drain regions are formed in the semiconductor substrate that separated by a channel region in the substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove portions of the insulating layer and the layer of silicon carbide of Halvis in forming the gate as taught by Tohyama, wherein forming diffused regions functioned as source and drain regions in the semiconductor substrate that separated by a channel region in the substrate is taught by Chamberlain. This is because of the desirability to control the desired thickness of the gate insulating layer, wherein thickness of each of the gate insulating layers are formed independently from each other, wherein source and drain regions are used for storing and transferring electrical charge.

Regarding other limitations including deposition techniques, for example, in claim 44, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting n-type or p-type dopants into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not

inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

Allowable Subject Matter

4. Claims 33,47,62,67,70,75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

*** Applicant's remarks filed January 04, 2002 have been fully considered but they are not persuasive.

** Applicant remarks (at remark filed 1/4/02, Page 2, third paragraph) that "...Halvis does not disclose forming a source region and a drain region...". This is noted and found unconvincing. This is a 35 USC 103 rejection, in which the main reference of Yamazaki clearly teaches to form source region 203 and drain region 204. As disclosed by Yamazaki at column 1, the memory device is also EPROM, in which the cell must be exposed to strong ultraviolet light in order for stored data to be erased. Accordingly, using the silicon carbide would improve light response and sensitive.

*** Applicant mainly remarks (at remark page 3) that "...If the gate G1 of Chamberlain were replace by the transparent gate of Halvis as suggested in the Office Action, the principle of operation of the device of Chamberlain would be changed, and it would be unsatisfactory for its intended purpose of detecting incident light".

In response, this is noted and found unconvincing. First, as noted by Applicant that, Chamberlain already teaches (at column 3, lines 39-44) that "...all parts of the photodetector are shield form light except for region D1...". Thus, the gate must be still shielded regardless of whether the gate is polysilicon or polysilicon-carbon. Accordingly, the principle of operation of the device of Chamberlain is still the same and would be satisfactory for its intended purpose of detecting incident light.

Second, Halvis clearly teaches (at col 3, lines 31-35) that "By adding carbon to the polysilicon material of a MOS photodetector device, the amount of visible light absorbed by the gate material can be reduced, and the quantum efficiency of the detector can thereby be improved". Thus, by employing this polysilicon-carbon gate in Chamberlain with a shielding film thereon, the amount of visible light absorbed by the gate material can be reduced further. Accordingly, the principle of operation of the device of Chamberlain is still the same and would be satisfactory for its intended purpose of detecting incident light, wherein the quantum efficiency of the detector can thereby be improved.

Applicant remarks (at remark page 5) that "Halvis discloses a photodetector with multiple gates. There is no teaching that only one of the Halvis gates comprising polysilicon and carbon...".

In response, first, the above rejected claims merely require to form a gate (e.g. claims 21,43,50,55, etc.). Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Second, claims 33,47,62,67,70 are objected as above.

Applicant remarks about Yamazaki and Halvis that "...structures are very different and operate in a different manner..." are noted and found unconvincing. Structure and operation of the gate of both devices are substantially the same. Replacing different materials in forming the gate would have been obvious to skill artisan. It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide compound $Si_{1-x}C_x$, as taught by Halvis et al. This is because of the desirability to improve response, to improve performance and light sensitivity.

Applicant's remarks (at remark page 5, last paragraph) that "...Yamazaki includes a thin insulator 105 of silicon carbide formed selectively on a part of the drain 104 shown in Figures 1B to 1D...".

In response, it is noted and found unconvincing since Yamazaki also teaches other device as shown in Figures 2A to 2D, in which "...Yamazaki discloses a memory cell with a source region 203, a drain region 204, a floating gate 208, and a control gate 210...", and in which by

forming the floating gate 208, as also shown in Figures 2D of Yamazaki, using the silicon carbide compound, $Si_{1-x}C_x$, as obviously taught by Halvis et al, the modified floating $Si_{1-x}C_x$ gate 208 is not the same material as the silicon oxide insulator 207 (col 3, lines 37-68).

****

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Regarding "...structures are very different and operate in a different manner...", *Kooi et al (4,113,515)* evidently teach his method is obviously applicable in fabrication of both a photodetector charge transfer device having a gate 7(figs 1-3; col 5), and a MOS device having a gate 93, source region and drain region (Figs 8-12; col 8, lines 31-68).

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner